

Post-Silicon Debug with JasperGold® Verification System

Formal Verification Unleashed!

Overview

Debugging silicon is a challenging task, one that creates urgency and stress within the SoC bring-up team. Production and time to market pressures demand fast turn-around time for this difficult problem. Formal methods are unique among EDA tools in tackling post-silicon bugs. JasperGold® Verification System formal verification platform tackles the problem due to its ability to resolve verification ambiguity for significant blocks with high level requirements. Since these complex properties are exactly the type used in post-silicon debug, JasperGold formal verification is unique in its ability to handle the associated capacity issues of silicon debug applications.

The Post-Silicon Debug Flow

Traditional post-silicon debugging consists of running system level simulations in the hope of reproducing the bug seen in silicon. This process is extremely inefficient. The bug cause must be hypothesized, including all inter-block timing dependencies for the bug. The symptom must propagate to an output port in order to verify the symptom matches the silicon bug. All of this must be accomplished by triggering only the top level inputs.

Formal post-silicon debug is much easier, faster, and far more effective than simulation for this purpose. The Jasper formal post-silicon debug flow is shown in Figure 1.

When a bug is detected, the team creates a property declaring the observed bad behavior should not exist. JasperGold formal verification will fail the property and generate a waveform describing the exact sequence of events to reproduce the observed bug. Because formal tests all possible input sequences, the analysis is not dependent upon guessing the correct vector to stimulate the bug. Formal provides the path for you.

With an appropriate property, JasperGold formal verification can find the bug in a mere fraction of the time it would normally take to diagnose the same bug in the lab or using emulation. This time may be weeks to months shorter than alternative solutions, helping to alleviate the crisis and uncertainty.

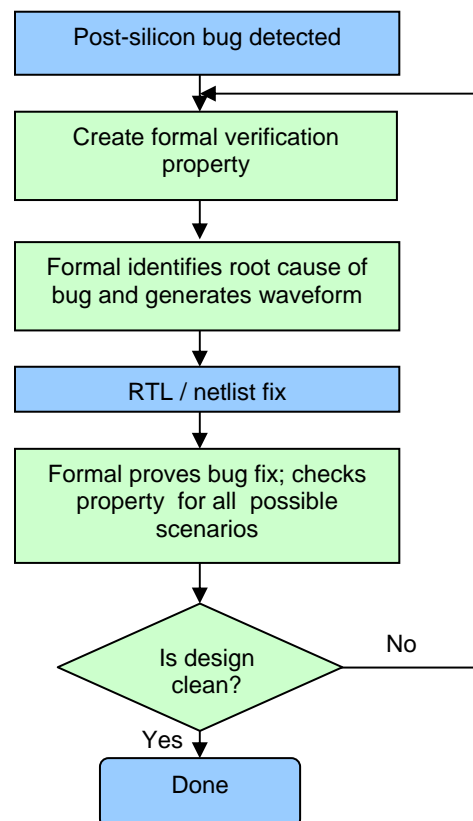


Figure 1 – Post-Silicon Debug Flow

Low level formal ABV tools are poorly suited to handling the large capacity of the debugging problems involved in post-silicon debug. Only JasperGold Verification System, a formal tool accommodating full proofs of complex design properties, has the capacity and methodology to effectively converge on the problem within demanding market window timelines. (See Figure 2.) First, JasperGold helps identify deeply embedded bugs quickly. Secondly, JasperGold can prove that the bug fixes to remove them are complete and have no other unintended side effects which violate the property being tested. It is being used regularly in production to identify issues several hundreds of clock cycles long on block level, end-to-end, high level properties. This unique ability makes it ideally suited for discovering the root cause of many deeply hidden post-silicon debug problems.

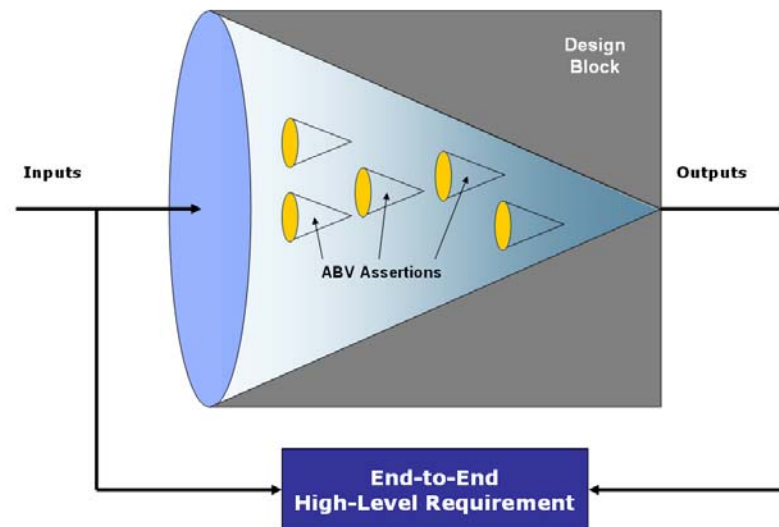


Figure 2 – ABV vs. High Level Properties

Summary

Naturally, avoiding silicon bugs is of paramount importance. Companies which use formal verification as a part of their design and verification flow significantly reduce the chance of bug escapes to silicon. The exorbitantly high cost of silicon bug escapes can be dramatically diminished by identifying the source early in the design flow. However, if a bug does slip through to silicon, JasperGold formal verification dramatically speeds up post-silicon verification and debug, and results in much higher confidence in the fix than alternative methods.

JasperGold Verification System is invaluable in reducing the time and effort spent addressing post-silicon debug issues. Its' high-capacity formal engines and proven deep formal methodology deliver a unique ability to quickly identify bugs, assure the integrity of sub-blocks, and verify the completeness of design fixes. This makes JasperGold the highest value post-silicon debug tool in the verification team's arsenal. JasperGold Verification System formal verification has the capacity and production-proven capability to tackle tough post-silicon debug and shorten turn-around time and time-to-market.