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Formal verification checks IC power reduction features

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With increasing densities and frequencies, power consumption has become a prevalent issue in design today. Dedicated power management schemes are designed into chips to conserve power consumed both statically and dynamically. Along with this comes the importance of verifying these power management schemes.

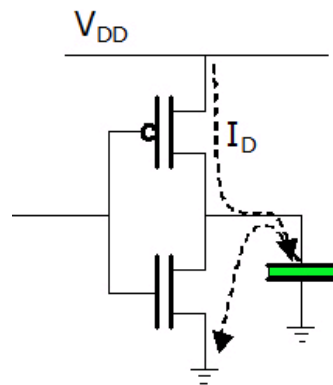
This article will examine the various issues and existing solutions surrounding the verification of power management schemes, and will discuss how SystemVerilog properties can be written for the formal verification of power management systems. This includes the verification of:

- Clock gating for power island power-down and power-up sequencing
- State and data retention
- Clock domain synchronization
- Clock domain data crossing synchronization

Lastly, this article will explore the emerging and evolving needs of IC designers facing ever-increasing consumer demands for greater speed and performance while balancing the need for power reduction now and in the future.

Types of power consumption

Traditionally, dynamic power has been the dominant concern for low-power CMOS design. Dynamic power (sometimes referred to as switching power) is the power consumed due to switching in the design. This power can be characterized as follows:



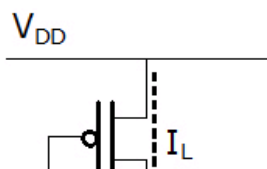
$$PD = CL * V_{dd}^2 * Freq$$

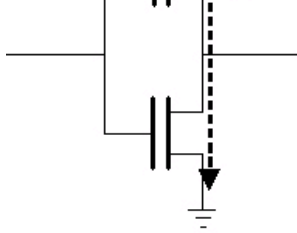
Figure 1 – Dynamic power

This power is directly proportional to the capacitance and frequency, and is proportional to the square of the voltage.

With the advancement of CMOS physical design, transistor channel widths have continued to shrink. With this comes the additional density of gates per square millimeter, as well as increased performance. Unfortunately, this has also caused a secondary element of power consumption, which has traditionally been ignored, but which has now become a dominant source of power consumption.

This secondary element is known as static or leakage power. It can be characterized as follows:





$$PS = V_{DD} * I_L$$

Figure 2 – Leakage power

Leakage power is the power consumed independently of switching in the design. In other words, leakage power is purely physical technology process dependent.

With gate channel widths greater than 90 nm, the leakage power consumption was minimal and could largely be ignored. With 90 nm gate channel widths technology, leakage power is approximately 30% of the power consumed.

With the latest 65 nm technologies, leakage power becomes the dominant power consumed in CMOS design. There is no easy formula to represent leakage power, but it is inversely proportional to the threshold voltage, which makes it directly proportional to performance, and it has a cubic dependency on V_{DD}. Therefore, as gate lengths get smaller, the power strategies must be devised to address static power consumption.

Methods of minimizing power consumption

There are some common methods for minimizing power consumption. Until recently, dynamic power was the focus in reducing overall power consumption. Despite lots of manual approaches, there are EDA tools available that focus on reducing the switching (or frequency) and reducing the voltage.

The most common approaches for reducing the switching are clock gating and data gating. The most common approach for addressing the voltage reduction involves manual/adaptive V_{DD} scaling, along with using voltage islands. For static power, the approaches are many: power gating, input vector control (leveraging the stack effect), reverse body bias (RBB), variable thresholds CMOS (MTCMOS), multiple thresholds CMOS (MTCMOS), variable supply voltage. Of these, power gating is the functional approach that is most effective at limiting standby leakage.

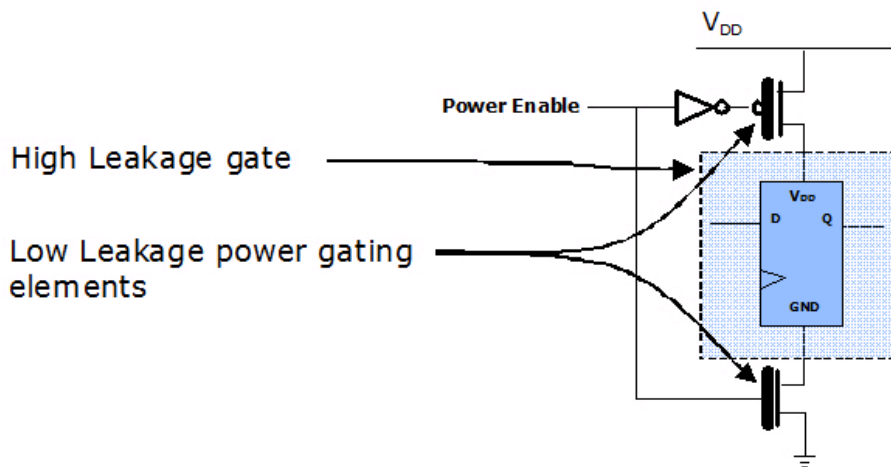


Figure 3 – Power gating

With each of these approaches, however, come risks to the functionality of the design. For instance, clock frequency scaling introduces the possibility of issues in clock domain crossing, whereas power gating introduces the problems of undriven signals and loss of state. As a result, the challenge of verifying a given power management strategy lies not only in verifying that the strategy itself is implemented as intended, but in verifying that its side effects don't adversely affect the overall functionality of the design.

The latter is by far the harder of the two tasks. With the addition of power management logic, it is possible to introduce unknown changes in functionality. Often these logical variances can manifest themselves in corner cases, so using traditional simulation-based verification can be inadequate to completely verify the design.

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